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1. http://www.ixpintel.nntu.nnov.ru/dokym_rykov/prim_kod_ixp1200/pdf/ReferenceDesign%:
... One per **Microengine**. Determine which Transmit Queues have packets ... Lookup next **hop** address. U move packet from RFIFO to packet buffer ...
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2. DiffServ over Network Processors: Implementation and Evaluation (PDF)
... 2K **instruction** headroom (named "control store") for each **microengine** ... Mouftah, "Performance Eval
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... can supply **instruction** source operands; when NN register is ... **microengine**, and each **microengine** t along with their next **hop** information ...
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4. Network processors: Guiding design through analysis (PDF)
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www.cs.wisc.edu/~kosart/papers/netproc.pdf - 239k - View as html - More from this site

6. NPU software taps virtual machine approach
However, the very strength of network processors — being a "soft" solution via software — is also the key new **instruction**-set architecture, address different ... packets, doing next-**hop** lookups on another set ... a per **microengine** ...
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... 16K B. **Instruction**. Cache. 8 K B ... StrongARM Core has access to all **Microengine** LOCAL_CSRs ... Microengines (**hop** = step from one context change ...
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High-level functional language let's designers express a wide variety of packet-processing applications. ... I different ... packets, doing next-**hop** lookups on another set ... a thousand per **microengine**), eight hardwa
commsdesign.com/design_library/cd/np/showArticle.jhtml?... - 48k - Cached - More from this site

9. EE Times -NPU software taps virtual machine approach
... have a new **instruction**-set architecture, address different ... packets, doing next-**hop** lookups on anoth threads per **microengine** ...
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10. http://www.gigascale.org/mescal/forum/81/mel.ppt (MICROSOFT POWERPOINT)
... memory lookups (4 threads per **microengine**) Currently no support ... processor, 128Kbyte L1 data and

latency per **hop** of 550 □sec ...
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... The byte_align **instruction** allows concatenation of data ... is addressable storage located in the **microengine**. ... with their associated next-**hop** forwarding information ...
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[PPT] Introduction to Network Processors
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... Applications: IPv4 Routing. Routers determine next **hop** and forward packets. ... IXP1200 **Microengine**. 4 hardware contexts. ... 4KB SRAM **instruction** stor – not a cache! ...
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... 1000 1996 1997 1998 1999 2000 2001 CPU Instructions per minimum length packet since 1996 ... IP Address Next **Hop** Queue ... Fine-grained parallelism: **instruction**-level ...
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... 1 always resolves the 'Next-**Hop**' route in ... languages for the StrongARM and **microengine** processors, the ... Plane microcode Receive: 472 instructions store size ...
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1 Hardware support for distributed objects in a hypercube

J. L. Kozarek

January 1988 **Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1**

Full text available: pdf(813.20 KB) Additional Information: full citation, abstract, references, index terms

A survey of parallel programs written for an experimental hypercube indicates that while systolic dataflow programs map well to a hypercube, general purpose programs with random dataflow are seriously constrained by the cost of communication. This paper proposes the augmentation of the hypercube architecture with a special-purpose communications coprocessor that provides hardware support for distributed objects. We anticipate this will increase the efficiency of inter-process commun ...

2 The design of nectar: a network backplane for heterogeneous multicomputers

Emmanuel Arnould, H. T. Kung, Francois Bitz, Robert D. Sansom, Eric C. Cooperm

April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems**, Volume 17 Issue 2

Full text available: pdf(1.73 MB) Additional Information: full citation, abstract, references, citings, index terms

Nectar is a "network backplane" for use in heterogeneous multicomputers. The initial system consists of a star-shaped fiber-optic network with an aggregate bandwidth of 1.6 gigabits/second and a switching latency of 700 nanoseconds. The system can be scaled up by connecting hundreds of these networks together. The Nectar architecture provides a flexible way to handle heterogeneity and task-level parallelism. A wide variety of machines can be connected as Nectar nodes ...

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1 **Asynchronous microengines for efficient high-level control**
Jacobson, I.; Gopalakrishnan, G.;
Advanced Research in VLSI, 1997. Proceedings., Seventeenth Conference on , 16 Sept. 1997
Pages:201 - 218

[Abstract] [PDF Full-Text (1220 KB)] IEEE CNF

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2 **The effect of frequency on the lifetime of a surface micromachined microengine driving a load**
Tanner, D.M.; Miller, W.M.; Eaton, W.P.; Irwin, L.W.; Peterson, K.A.; Dugger, Senft, D.C.; Smith, N.F.; Tangyunyong, P.; Miller, S.L.;
Reliability Physics Symposium Proceedings, 1998. 36th Annual. 1998 IEEE International , 31 March-2 April 1998
Pages:26 - 35

[Abstract] [PDF Full-Text (2692 KB)] IEEE CNF

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Sniegowski, J.J.; Garcia, E.J.;
Electron Device Letters, IEEE , Volume: 17 , Issue: 7 , July 1996
Pages:366 - 368

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4 **MEMS reliability in a vibration environment**
Tanner, D.M.; Walraven, J.A.; Helgesen, K.S.; Irwin, L.W.; Gregory, D.L.; Sta J.R.; Smith, N.F.;
Reliability Physics Symposium, 2000. Proceedings. 38th Annual 2000 IEEE

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7 **Effect of W coating on microengine performance**
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8 **Fluidic packaging of microengine and microrocket devices for high-pressure and high-temperature operation**
Peles, Y.; Srikar, V.T.; Harrison, T.S.; Protz, C.; Mracek, A.; Spearing, S.M.;
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Melear, C.;
Southcon/95. Conference Record , 7-9 March 1995
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Hwu, W.W.; Patt, Y.N.;
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12 **Bent-beam electrothermal actuators-Part II: Linear and rotary microengines**
Jae-Sung Park; Chu, L.L.; Oliver, A.D.; Gianchandani, Y.B.;
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Schanwald, L.P.; Schwank, J.R.; Sniegowsi, J.J.; Walsh, D.S.; Smith, N.F.; Peterson, K.A.; Shaneyfelt, M.R.; Winokur, P.S.; Smith, J.H.; Doyle, B.L.;
Nuclear Science, IEEE Transactions on , Volume: 45 , Issue: 6 , Dec. 1998
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14 **Development of Si-SiC hybrid structures for elevated temperature micro-turbomachinery**
Hyung-Soo Moon; Dongwon Choi; Spearing, S.M.;
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15 **An electrostatic, on/off microvalve designed for gas fuel delivery f the MIT microengine**
Xue'en Yang; Holke, A.; Jacobson, S.A.; Lang, J.H.; Schmidt, M.A.; Umans, S.
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Pages:660 - 668

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Chapter 2 The Ixp12xx Programming Environment - The Goal Of (Correct)
compiler. What you discovered was that the **microengines** don't run any operating systems, and the C StrongARM* core{ XE "StrongARM core" and six **microengines** all on the same die. The StrongARM core is an www.intel.com/intelpress/ixp1200/ixp-chapter.pdf

Performance Analysis of the Intel IXP1200 Network Processor - Http (Correct)
and six programmable RISC cores (also known as `**microengines**'The core runs the VxWorks operating system the VxWorks operating system and controls the **microengine** threads. Each **microengine** can execute up to core uses these registers to program, control, and **debug** the **microengines**. Each **microengine** instruction is gs129.sp.cs.cmu.edu/papers/15740f00-ixp1200.ps

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